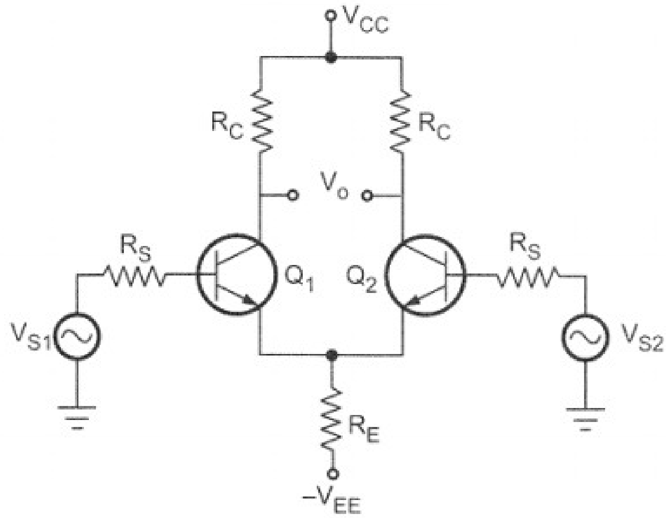
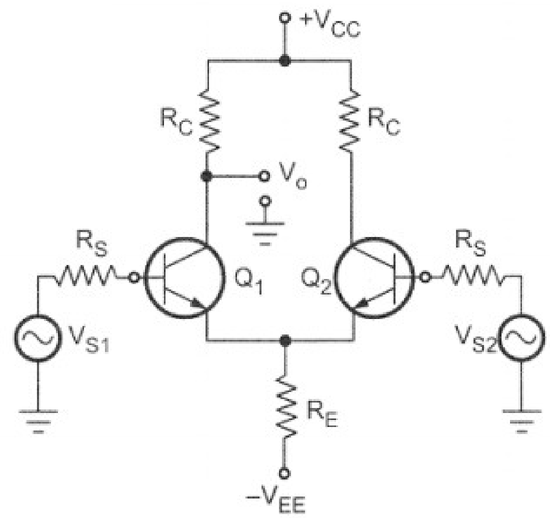
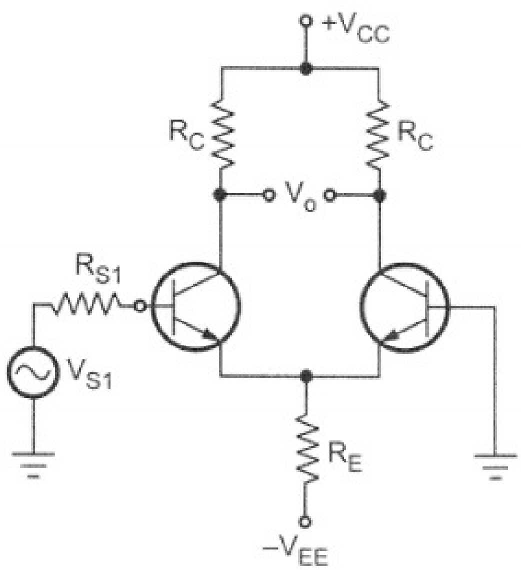
Basic Concept of Differential Amplifier



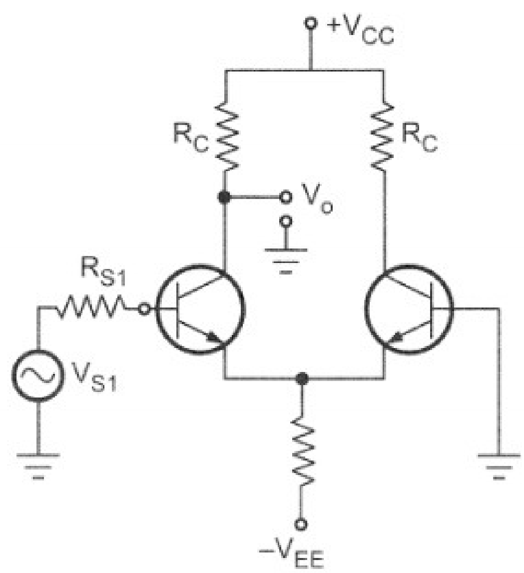
(a) Dual input balanced output



(b) Dual input unbalanced output



(c) Single input balanced output



(d) Single input unbalanced output

A differential amplifier is a type of electronic amplifier which multiplies the difference between two inputs by some constant factor. It is the basic building block of an OPAMP. The two transistors Q_1 and Q_2 have identical characteristics. The intensity of $+V_{CC}$ is equal to the intensity of $-V_{EE}$. These voltages are measured with respect to ground. Ideally, the output voltage is zero when the two inputs are equal. In an equation form, $V_0 \propto V_{S1} \sim V_{S2}$.

There are four configurations of a differential amplifier, shown in Figure 1.

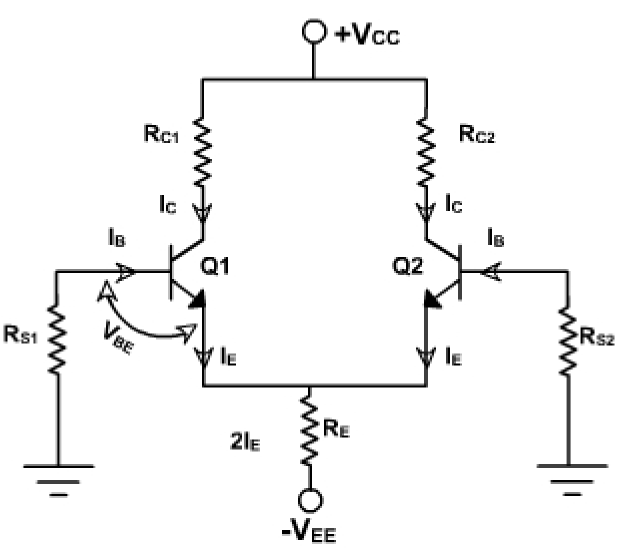
(a) Dual input balanced output differential amplifier
The signal is given to both the input terminals
The output is taken between the two collectors

(b) Dual input, unbalanced output differential amplifier.
The signal is given to both the input terminal
The output is taken from one collector with respect to ground

(c) Single input, balanced output differential amplifier.
The signal is given to only one input terminal and other terminal is grounded
The output is taken between the two collectors

(d) Single input, unbalanced output differential amplifier
The signal is given to only one input terminal and other terminal is grounded
The output is taken from one collector with respect to ground

DC Analysis of a Dual input – Balanced Input Differential Amplifier



Since the emitter biased part is common for both the sections as shown in Figure 2, therefore determining the operating point for only one section will be applicable for both the sections.

As the value of R_{S1} and R_{S2} are equal, let us take $R_{S1} = R_{S2} = R_S$.

Applying KVL in the base emitter loop of the first section,

$R_S I_B + V_{BE} + 2I_E R_E = V_{EE}$ (1)

But, $I_B = I_C / \beta_{dc}$ and $I_C \approx I_E$.

Therefore, $R_S I_C / \beta_{dc} + V_{BE} + 2I_E R_E = V_{EE}$

Or, $I_C = I_E = (V_{EE} – V_{BE}) / (2R_E + R_S / \beta)$

Generally, $R_S / \beta_{dc} << 2R_E$ as R_S is the internal resistance of the input signal.

Therefore, $I_C = I_E = (V_{EE} – V_{BE}) / 2R_E$ (2)

Again, $R_{C1} = R_{C2} = R_C$.

Applying KVL in the collector-emitter loop,

$V_{CC} = I_C R_C + V_{CE} + 2I_E R_E - V_{EE}$

Or, $V_{CE} = V_{CC} - I_C R_C – (2I_E R_E - V_{EE})$ (3)

Now, if R_S is negligible, from (1),

$V_{BE} = 2I_E R_E - V_{EE}$ (4)

Thus, applying (4) in (3) we get,

$V_{CE} = V_{CC} - I_C R_C – V_{BE}$

Or, $V_{CE} = V_{CC} - V_{BE} - I_C R_C$ (5)

I_{CQ} and V_{CEQ} can be determined from (2) and (5) respectively.

Constant Current Bias

In the DC analysis of the differential amplifier, it was observed that emitter current I_E depends on the value of the β. To make the operating point stable, I_E current should be constant irrespective of the value of β. To avoid the effect of β, R_E should be quite large. But a large value of R_E in turn decreases the current I_E and then, to maintain the same value of I_E, emitter supply V_{EE} should be increased. But as it is not a practical way out, another technique, called the current bias is used.

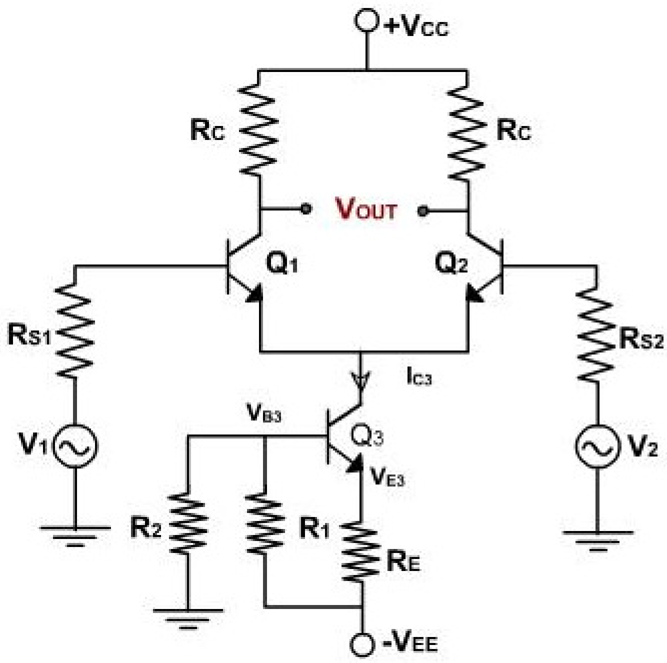


Figure 3 shows dual input balanced output differential amplifier by using a constant current bias. The resistance R_E can be replaced by the constant current transistor Q_3. The DC collector current in Q_3 can be established by R_1, R_2, & R_E.

By applying the voltage divider rule, the voltage at base of Q_3 is

$$V_{B3} = \frac{R_2}{R_1 + R_2} (-V_{EE})$$

$$V_{E3} = V_{B3} - V_{BE3}$$

$$= -\frac{R_2}{R_1 + R_2} V_{EE} - V_{BE3}$$

$$I_{BE3} = I_{C3} = \frac{V_{E3} - (-V_{EE})}{R_E}$$

$$= \frac{V_{EE} - \left(\frac{R_2}{R_1 + R_2}\right) V_{EE} - V_{BE3}}{R_E}$$

As the two halves of differential amplifiers are symmetrical, each has half of the current I_{C3}.

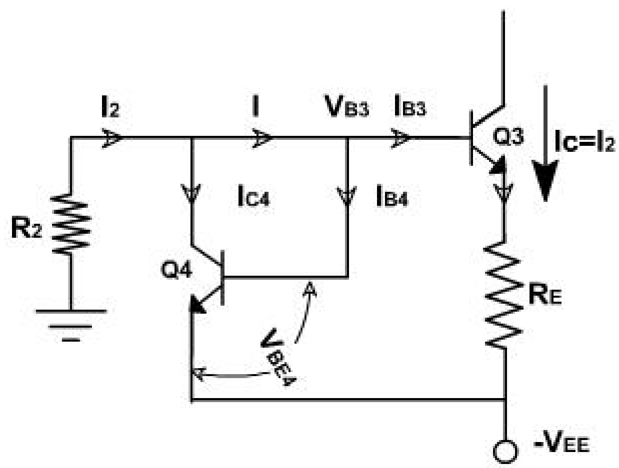
$$I_{E1} = I_{E2} = \frac{I_{C3}}{2} = \frac{V_{EE} - \left[\frac{R_2}{R_1 + R_2} V_{EE}\right] - V_{BE3}}{2R_E}$$

The collector current, I_{C3} in transistor Q_3 is fixed as no signal is injected into either the emitter or base of Q_3.

Besides supplying the constant emitter current, constant current bias provides a very high source resistance also since the AC equivalent or DC source is ideally an open circuit.

Current Mirror

The circuit in which output current is forced to equal the input current is said to be a current mirror circuit. Therefore in a current mirror circuit, the output current is a mirror image of input current. The current mirror circuit is shown in the figure 4.



The current mirror is the special case of constant current bias. The current mirror bias requires few components than the constant current bias circuits.As Q_3 and Q_4 are identical transistors,

$$V_{BE3} = V_{BE4}$$

$$I_{B3} = I_{B4}$$

$$I_{C3} = I_{C4}$$

Summing currents at node V_{B3}

$$I_2 = I_{C4} + I$$

$$= I_{C4} + 2I_{B4} = I_{C3} + 2I_{B3}$$

$$= I_{C3} + 2\left(\frac{I_{C3}}{\beta_{dc}}\right)$$

$$= I_{C3}\left(1 + \frac{2}{\beta_{dc}}\right)$$

Generally β_{dc} is large enough, therefore $2/\beta_{dc}$ is small.

$$\therefore I_2 \approx I_{C3}$$

$$I_2 = \frac{V_{EE} + V_{BE3}}{R_2}$$